What is the HSV board and what does it do ?

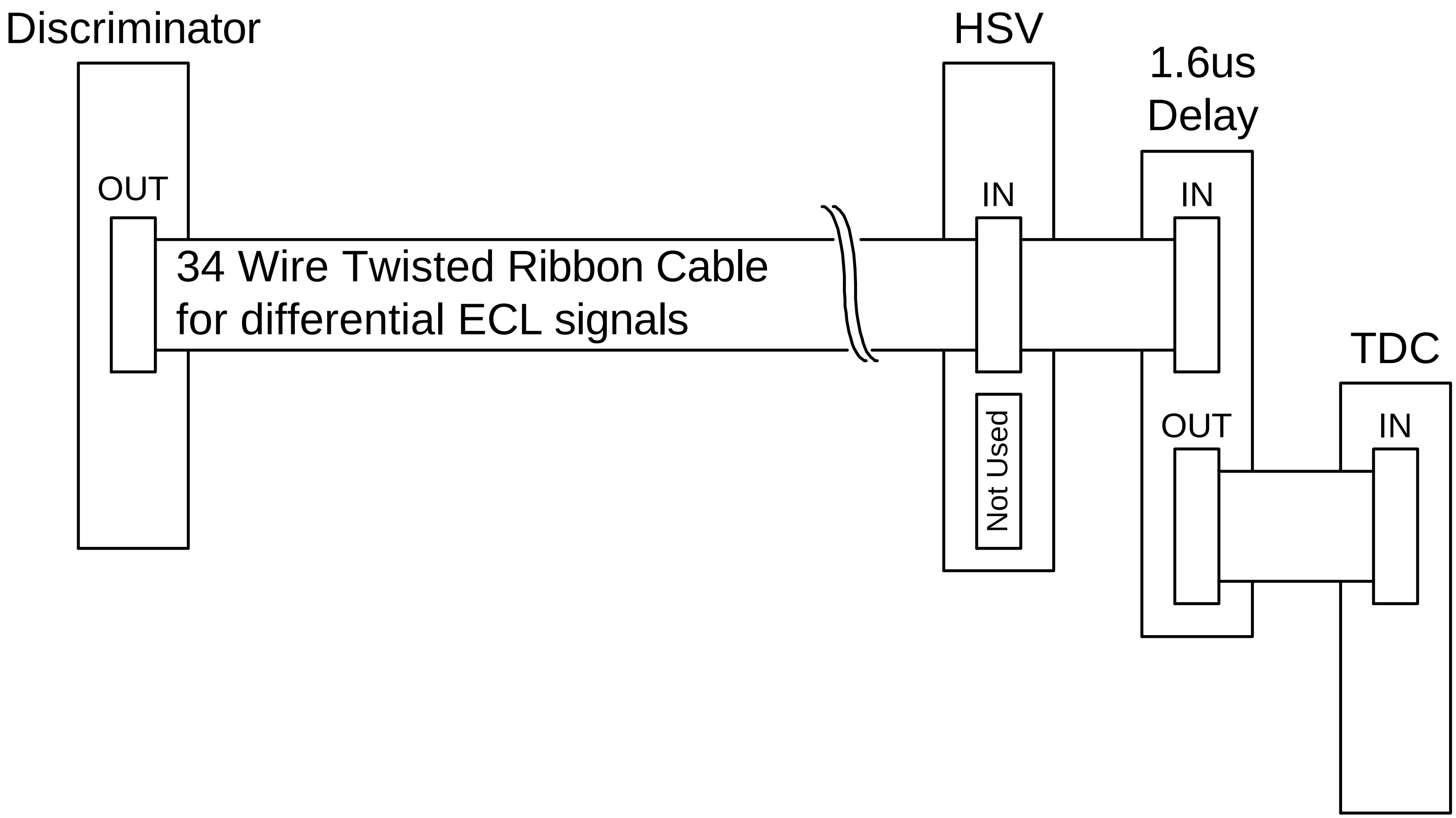
- Designed to intercept the old trigger, compare event to list of known bad events, and reject known bad events and let the rest pass.

- Designed to make those decisions in a very short timeframe so this board can work with the rest of the current DAQ hardware.

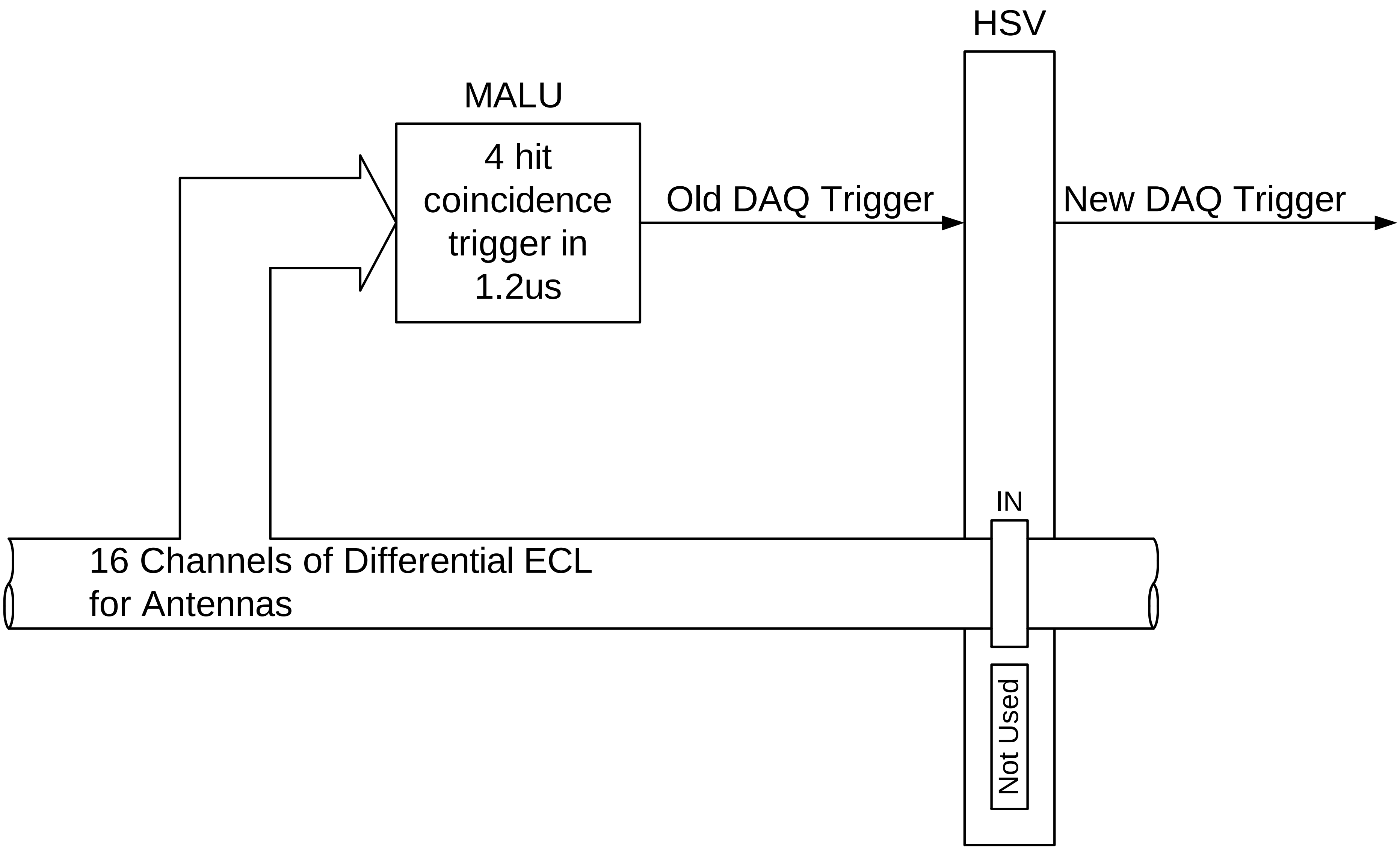
- Designed to be provisionable so that in the field the scientist can change the operating parameters to meet whatever conditions they meet or experiments they want to try.

- Designed to gather status data and report that data to a user interface which will log data to give scientists a good idea how the system is performing.

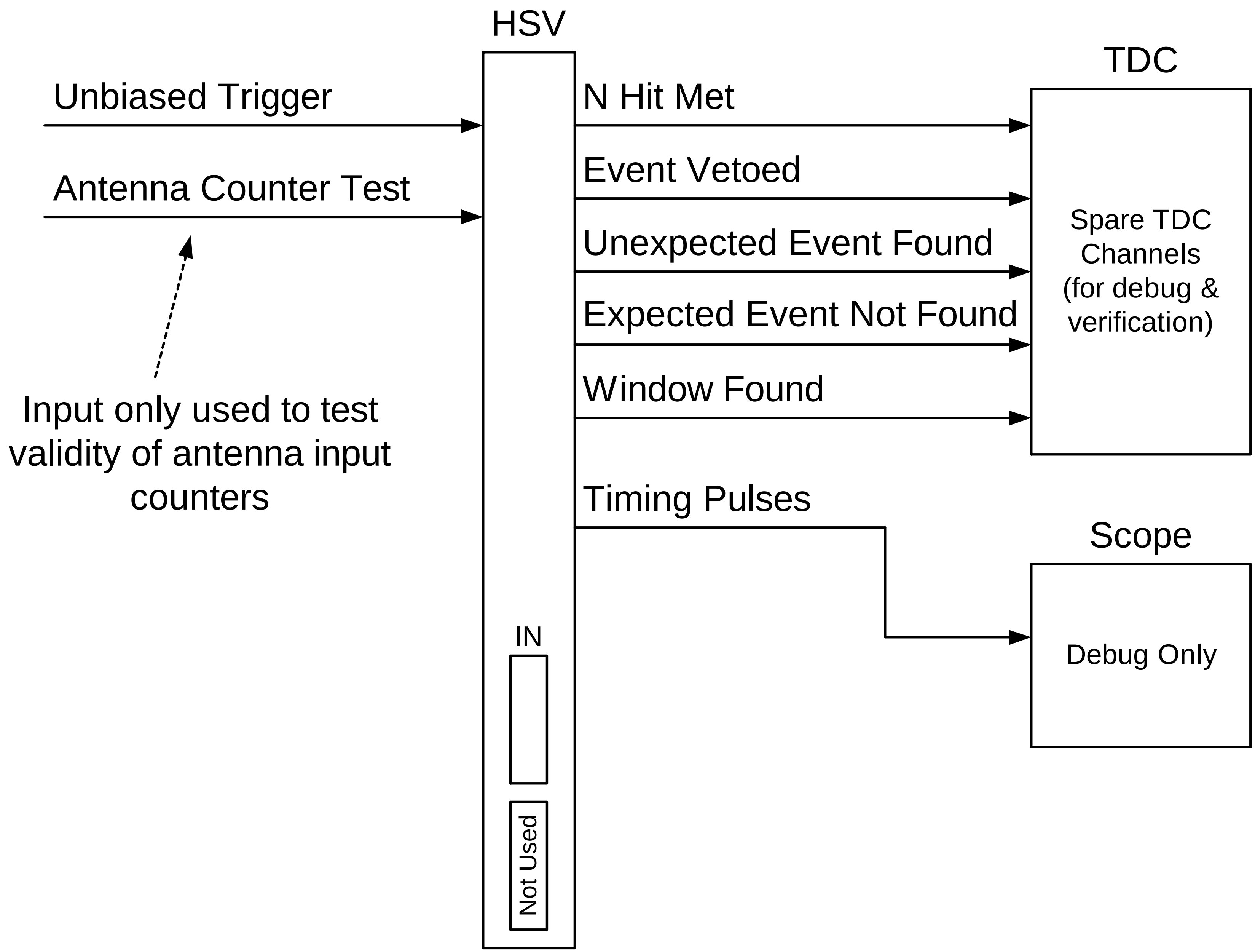
Antenna Data Connections



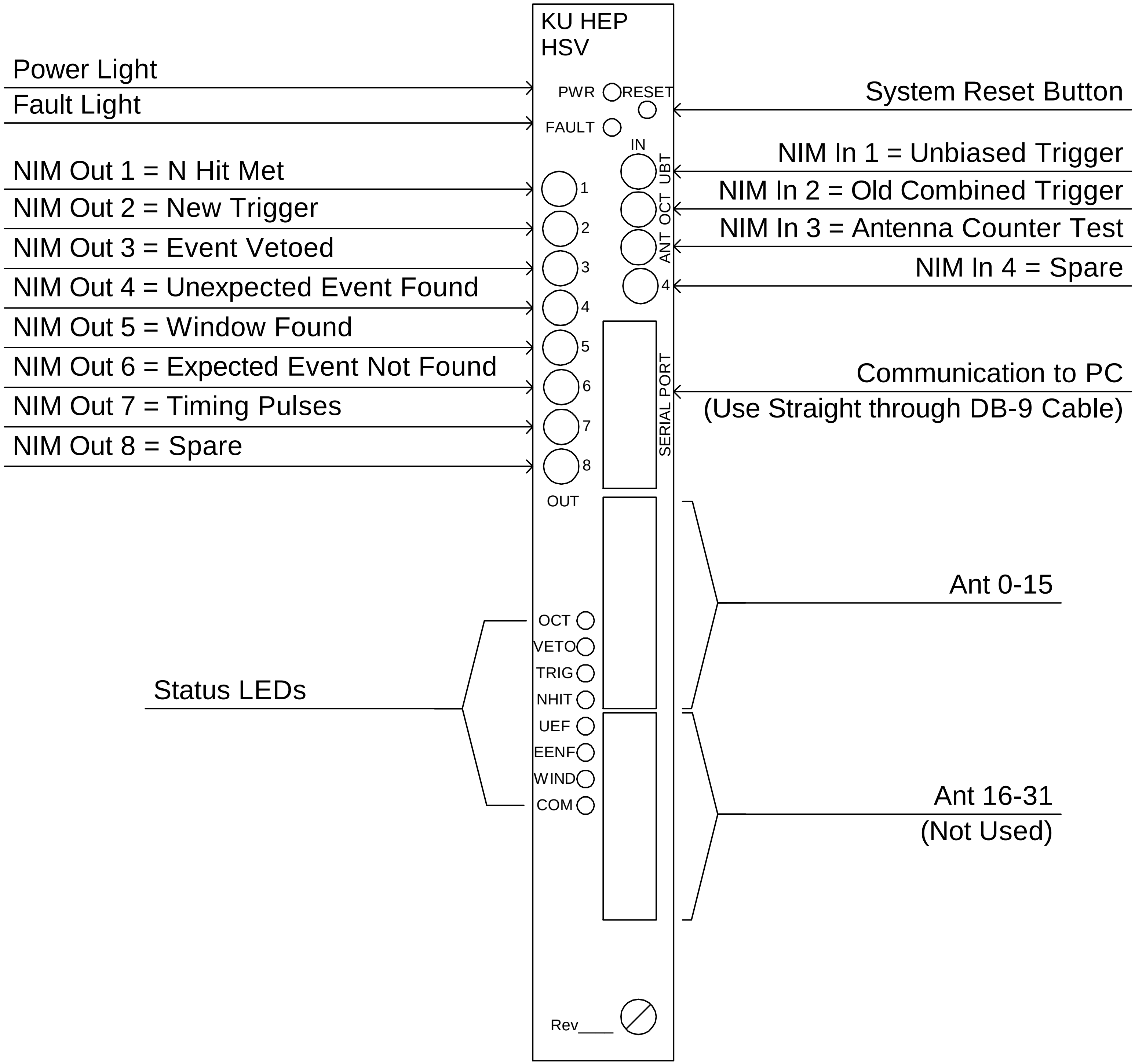
Trigger Connections



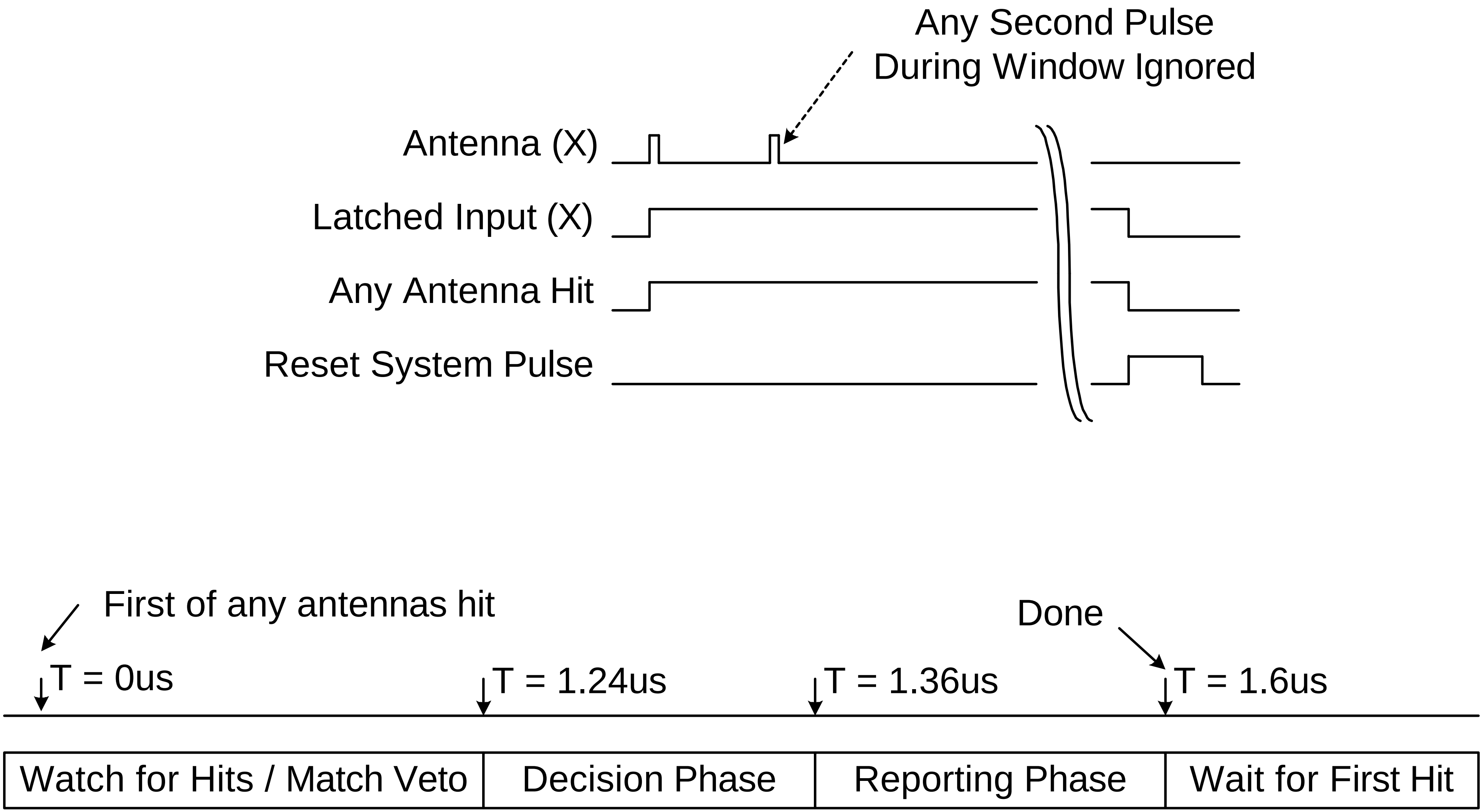
Other Connections



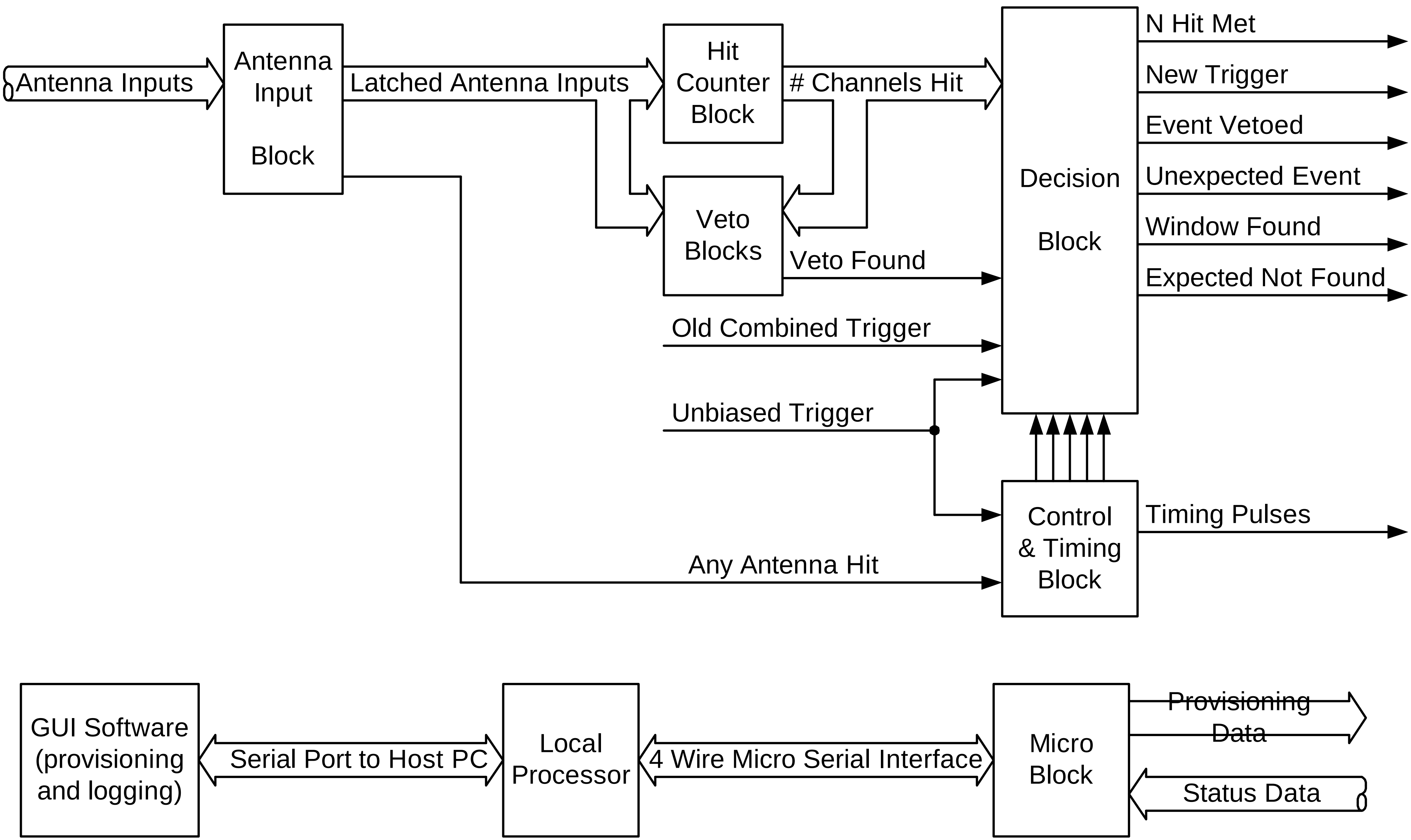
Front Panel Layout



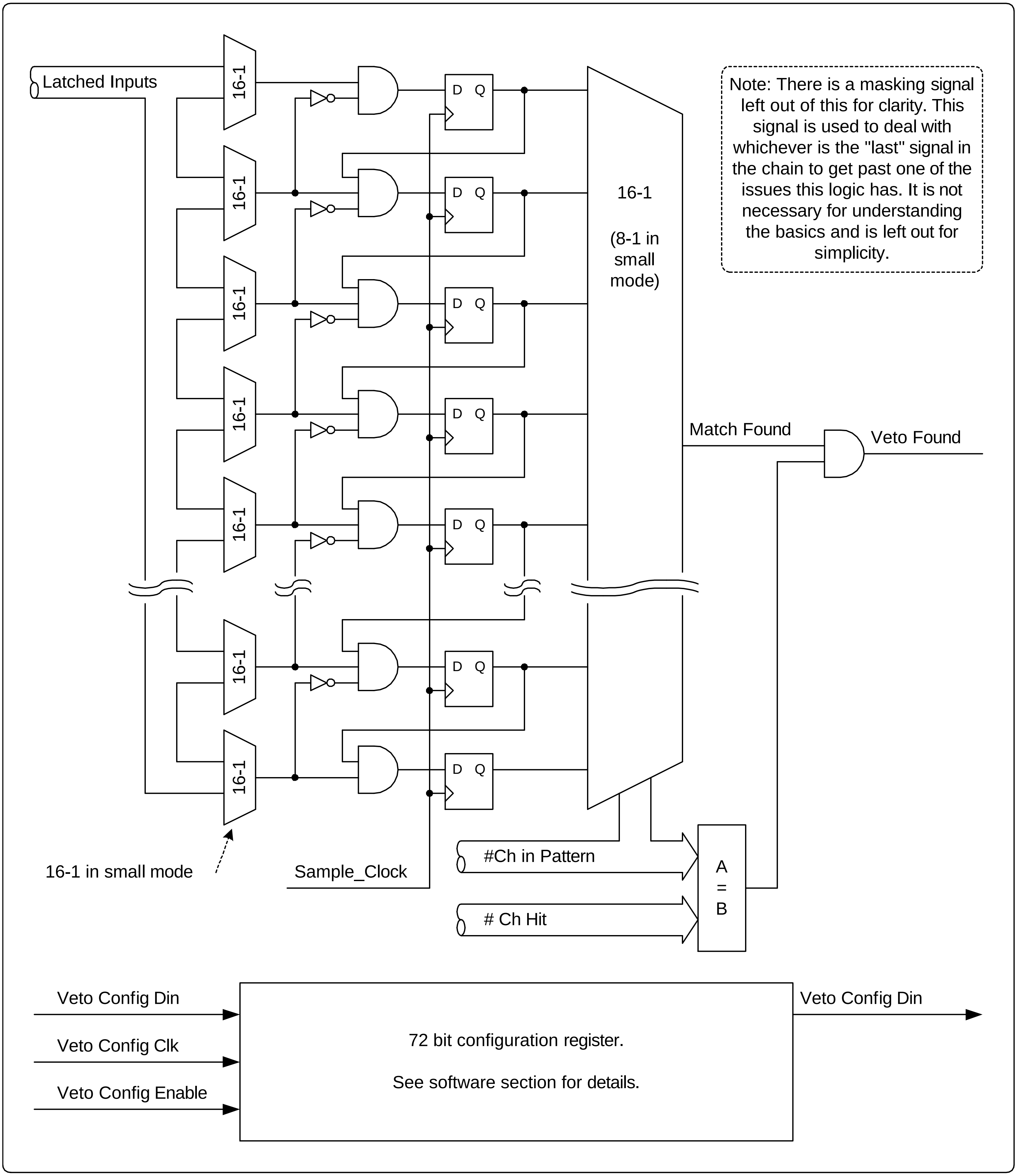
System Timing

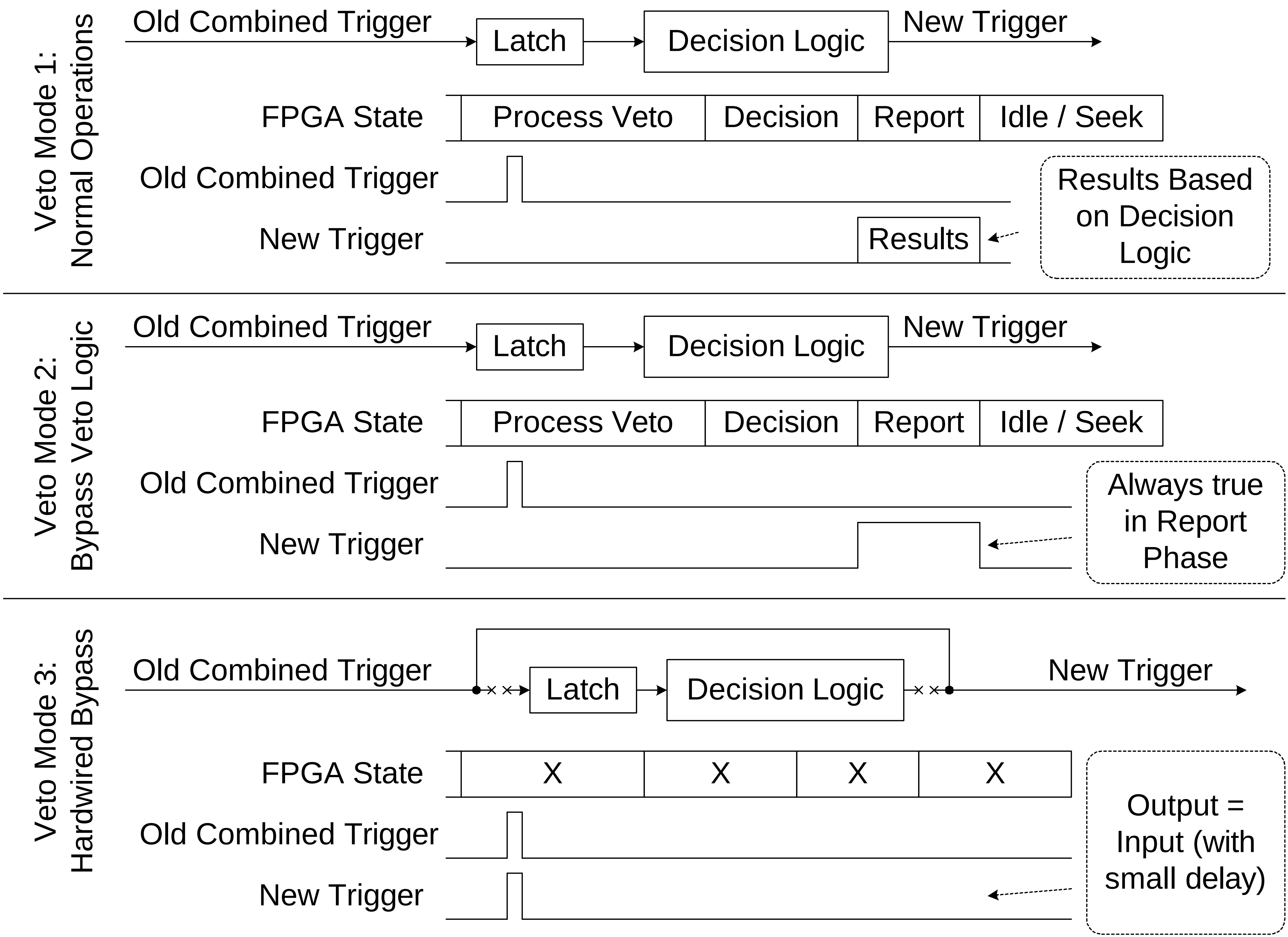


Very Simple Block Diagram



Veto Block Details





Veto Mode 1:
Normal Operations
Old Combined Trigger
Latch
Decision Logic
New Trigger
FPGA State
Process Veto
Decision
Report
Idle / Seek
Old Combined Trigger
New Trigger
Results
Results Based on Decision Logic
Veto Mode 2:
Bypass Veto Logic
Old Combined Trigger
Latch
Decision Logic
New Trigger
FPGA State
Process Veto
Decision
Report
Idle / Seek
Old Combined Trigger
New Trigger
Always true in Report Phase
Veto Mode 3:
Hardwired Bypass
Old Combined Trigger
Latch
Decision Logic
New Trigger
FPGA State
X
X
X
X
Old Combined Trigger
New Trigger
Output = Input (with small delay)

GUI Slides

Insert some screen slides about GUI here. Ken will make.

Status Data

Every 10ms, the FPGA sends data to the local processor. The local processor collects and adds the data for 100 samples and every 1 second sends that data to the PC where the GUI deals with logging.

The counters are sized as small as reasonable to reduce the number of gates used and allow for more veto blocks.

Counting are we counting ?	# of Bits	Max count / 10ms period	Max Avg Frequency
Each Antenna Input (16)	16	65,536	6.55 MHz
Unbiased Trigger Input	2	4	400 Hz
N Hit Met Signal	13	8,192	819 KHz
NHit, but UEF	13	8,192	819 KHz
NHit, but Prescalled	13	8,192	819 KHz
"Hot" Veto Channels (3)	13	8,192	819 KHz
"Medium" Veto Channels (5)	10	1024	102.4 KHz
"Other" Veto Channels (17)	4	16	1.6 KHz

Deadtime Improvements

- Very important to remember we do not have good data from pole yet.
- Old DAQ software pre-veto took 50ms to compute. If 100Hz noise present, then there would be 500ms of dead time.
- New system has a fixed deadtime of around 100ns to make decisions for each event window. There is a maximum window rate of 833kHz with the expected operating parameters.
- Very very difficult to compare deadtime numbers between old and new system. Will leave that for the physicists :)

Possible Future Improvements

- With same DAQ setup and decision time requirements, there is not a lot more that can be done on the fundamental architecture of the HSV (i.e. the decision time limit).
- Improvements could be made in sampling rate (i.e. redesign for faster FPGAs or use custom ASICs that can run much faster, both extremely expensive options).
- Could re-design to get more veto blocks now that we have a good idea what it takes to make a veto block (different & more FPGAs, multiplexer chips, etc).
- Could consider a fundamentally new design for a new flexible veto block, one that can do partial pattern matching and can handle more than one channel in a sample period.
- Extend system back to 32 input channels to accommodate more future antennas. Will not happen in current hardware unless you only need 5 veto blocks.

HSV Test Setup at the IDL at KU